Outline

• Motivation and Purpose
• System Versus Chip ESD
• The ESD Standards Gap
• Polymer Voltage Suppressor Characterization
• Bridging Standards Gap with TLP: GaAs RF Switch
• TLP for OEM Cable ESD
• Summary/Future
Motivation and Purpose

• ESD Characterization of POLYMER VOLTAGE SUPPRESSORS (PVS)

• A TLP method for specifying PVS products to improve Electronic Products:
  — Reliability
  — Mean time before failure
  — ESD Compliance
Motivation and Purpose

• Use of TLP to Bridge the Gap Between Chip and System level ESD Standards

• Increase the use of TLP for ESD equivalent test for:
  — System level ESD Failure Voltage
  — Cable ESD Failure Voltage
  — ESD Compliance using PVS components
System Level ESD Constraints

• Driven by:
  – Smaller semiconductors
  – High frequencies
  – Escalating numbers of signal lines

• ESD is a performance bottleneck
  – Limited chip area and board space
  – Capacitance loads
Industry ESD Constraints

• ESD is getting worse
  ─ On chip protection is failing system level ESD

• RF products need reliability:
  ─ Cell phones
  ─ SiGe applications
  ─ GHz servers
  ─ GaAs RF switches
  ─ VCSEL applications

• There is a gap between chip and board level ESD
  ─ 8 kV IEC has 6X more current than 8 kV HBM
Historically Chips were tested at 2000 V
  - 2000 V HBM = 1.3 Amp
  - 1.3 Amp is equivalent to 439 V IEC

Now: 8 kV IEC is equivalent to 36 kV HBM
8 kV IEC = 24 Amp versus 5.3 Amp HBM
That is the problem

TLP bridges the gap
The Standards Gap: On Chip Versus IEC

TLP Bridges the Gap: TLP Correlates to Both

Historical Trend

TLP Bridges the Gap: TLP Correlates to Both
PVS Fits RF ESD Constraints

- Capacitance < 150 fF
- Multiple line ESD protection
- Bipolar
- Low profile, ≤10 mils (0.25 mm)
- Pico-second ESD response
- Zero board space on a connector
- Substrateless Surface Mount
Polymer Voltage Suppression Devices

Substrateless Surface Mount Device

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EPI-FLO™ PVS 0603 Surface Mount Device Capacitance
TLP Component Testing

ESD Signal Generator

DUT

Signal Attenuator

8 GSa / Second Digital Oscilloscope

TLP set-up for PVS and RF components
Surface Mount Voltage Characterization

- **Vtrig**: Voltage is increased until device turns on
- **Endurance**: 20x at 600V ~ equivalent to 8kV IEC

<table>
<thead>
<tr>
<th>Device</th>
<th>Endurance Test</th>
<th>Vtrig Response</th>
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<td>Vtrig</td>
<td>600V 20th pulse, Vclamp</td>
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100, 200, 400 Vtrig Devices
TLP PVS Trigger Characterization

200 Volts input

4 ns, 38V

Vclamp

36 ns, 24V

200 Vtrigger 0603 Device
600 V TLP PVS Characterization

600 V, 20X Endurance Test

Volts (100V/div)

Time (10ns/div)

Vclamp

4 ns, 37V

36 ns, 27V

TLP .6 kV Equivalence to 8 kV IEC 6-10004-2
TLP/ESD System Testing

ESD Gun is Added to TLP Testing for Correlation
GaAS RF Switch Tested With and Without PVS
TLP/ESD Test for GaAs RF Switch

IV Trace: Post ESD/TLP damage to switch is change in leakage current when device is powered.

TLP/ESD gun Voltage Input on signal line with and without PVS device protection.
Step 1: GaAs RF Switch ESD Gun

- Zap Gun: IEC 6-10004-2
- Power device
- 10% Change in current at RFC = damaged device

<table>
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<tr>
<th>Vin</th>
<th>Pulse #</th>
<th>I (µA)</th>
<th>I (RFC) (µA)</th>
<th>I (RFC1) (µA)</th>
<th>I (RFC2) (µA)</th>
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Step 1: ESD Gun Test GaAs RF Switch

- **Pulse**
  - 1X, 5X, 10X, 20X
  - Ramp V by 100V

- **Failure = 10% change in RFC current**

*Failed Current < 253 µA*
Step 2: TLP Test GaAs RF Switch

- Pulse
  - 1X, 5X, 10X, 20X
  - Ramp V by 100V

- Failure = 10% change in RFC current

Failed Current = 158 µA
Final Step: 8 kV IEC Test with PVS

- Select PVS device $V_{trig} < 200$V
- Solder PVS device on board
- Zap 20x+ at 8 kV for ESD compliance

20 Pulses = IEC Requirement

GaAs Switch With 100Vtrig PVS Undamaged

Failure = 158 µA
**TLP Test Method Summary**

1. **IEC Unprotected Switch Failure 400V**
2. **TLP Unprotected Switch Failure 200V**
3. **PVS Protected Switch passes 50 8kV IEC pulses**

- **minizap**
- **TLP**
- **Minizap w EPI-Flo™**

Voltage In

Current Output

1 10 100 1000 10000
VCSEL HBM/TLP Test Result

<table>
<thead>
<tr>
<th>Initial Voltage</th>
<th>Current In</th>
<th>Current Out</th>
<th>V4ns</th>
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Photo Diode Current Output Showed PVS with Vtrig < 60 V Required for 1000 V HBM
Cable ESD Tests Need Standards

- Cable ESD varies:
  - Automotive:
    - 25 kV IEC
    - 10 kV TLP
  - Giga bit server:
    - 600 foot cable charged to 3kV

600V TLP test of RJ-45 connector with Magnetics shows no protection
Cable ESD PVS Specs ≠ IEC ESD

For Cable ESD for Server application, PVS Device on RJ-45 connector needs to be tested with 600 foot cable charged to 3 kV.

PVS installed on RJ-45 removes ~80% of 8 kV equivalent ESD TLP pulse.
The Future

• Low Capacitance PVS devices remove performance barriers for:
  — Cell phones, Giga bit servers, PDA’s
  — SiGe, GaAs, InP, semiconductors
  — Tunneling Magneto Resistive Heads

• PVS devices open doors for future sensitive semiconductors removing ESD as a potential barrier to Market entry
Summary

• The gap between chip and system level ESD standards needs a TLP standard

• TLP/ESD characterization using femto Farad Polymer Voltage Suppression devices provides 8 kV IEC reliability for RF products and components

• PVS devices open the door for future sensitive semiconductors removing ESD as a potential barriers to Market entry